Response to the PCT Written Opinion

1) The following comments were provided by the Examiner in the PCT Notice dated May 25, 2004:

A) Although claims 1-10, 14 and 15 possess novelty and inventive step, claims 11-13 do not possess novelty and inventive step based on Document 1 and Document 2.

As the reason for not possessing inventive step, the Examiner indicated that "the constitution specified by the manufacturing method is unclear, and, as a result, the invention is the same as Document 1 or Document 2 describing a semiconductor element wiring having a Cu seed layer formed on the TaN barrier film". The Documents are as follows:

JP2002-4048

JP2001-284358

B) The constitution of substances in claims 11-13 is unclear.

C) Although Comparative Example 4 is an invention pertaining to claim 1, the film thickness uniformity is not improved.

D) The sheet resistance is not described in the Examples and Comparative Examples.

2) The indication of foregoing A) to D) of the present invention being the same as Document 1 and Document 2, and other comments seem to be mostly based on typographical errors or insufficient explanations. Thus, the relevant descriptions have been corrected for accurate understanding.

The reason for this is now explained. Incidentally, for the sake of convenience of explanation, the amended claims are indicated once again below.

[Claims]

1. A copper alloy sputtering target containing 0.01 to (less than) 0.5wt% of at least 1 element selected from Al or Sn, and containing either Mn or Si or both in a total amount of 0.25wtppm or less.

2. A copper alloy sputtering target containing 0.05 to 0.2wt% of at least 1 element selected from Al or Sn, and containing Mn or Si in a total amount of 0.25wtppm or less.

3. A copper alloy sputtering target according to claim 1 or claim 2, further containing one or more selected from among Sb, Zr, Ti, Cr, Ag, Au, Cd, In and As in a total amount of 1.0wtppm or less.

4. A copper alloy sputtering target according to claim 1 or claim 2, further containing one or more selected from among Sb, Zr, Ti, Cr, Ag, Au, Cd, In and As in a total amount of 0.5wtppm or less.

5. A copper alloy sputtering target according to claim 1 or claim 2, further containing one or more selected from among Sb, Zr, Ti, Cr, Ag, Au, Cd, In and As in a total amount of 0.3wtppm or less.

6. A copper alloy sputtering target according to any one of claims 1 to 5, wherein the inevitable impurities excluding gas components are 10wtppm or less.

7. A copper alloy sputtering target according to claim 6, wherein the inevitable impurities excluding gas components are 1wtppm or less.

8. A copper alloy sputtering target according to any one of claims 1 to 7, wherein Na and K are respectively 0.05wtppm or less; U and Th are respectively 1wtppb or less; oxygen is 5wtppm or less; nitrogen is 2wtppm or less; and carbon is 2wtppm or less.

9. A copper alloy sputtering target according to claim 8, wherein Na and K are respectively 0.02wtppm or less; U and Th are respectively 0.5wtppb or less; oxygen is 1wtppm or less; nitrogen is 1wtppm or less; and carbon is 1wtppm or less.

10. A copper alloy sputtering target according to any one of claims 1 to 9, wherein the average crystal grain size is 100 μm or less, and the average grain size variation is within ±20%.

11. (Amended) A semiconductor element wiring formed with the sputtered film of a copper alloy sputtering target containing 0.01 to (less than) 0.5wt% of at least 1 element selected from Al or Sn, and containing either Mn or Si or both in a total amount of 0.25wtppm or less.

12. (Added) A semiconductor element wiring formed with the sputtered film of a copper alloy sputtering target containing 0.01 to (less than) 0.5wt% of at least 1 element selected from Al or Sn, and containing either Mn or Si or both in a total amount of 0.25wtppm or less; and further containing one or more selected from among Sb, Zr, Ti, Cr, Ag, Au, Cd, In and As in a total amount of 1.0wtppm or less.

13. (Amended) A semiconductor element wiring according to claim 11 or claim 12 formed as a semiconductor element wiring seed layer.

14. (Amended) A semiconductor element wiring according to claim 13 formed as

a seed layer on a barrier film of Ta, Ta alloy or the nitrides thereof.

15. (Amended) A manufacturing method of a copper alloy sputtering target according to any one of claims 1 to 10, comprising the steps of preparing a mother alloy as the additional element; melting this in a molten metal of copper or low concentration mother alloy to form an ingot; and processing this ingot to form a target.

16. A manufacturing method of a copper alloy sputtering target according to claim 14, wherein a mother alloy within the solid solubility limit is prepared.

3) Foremost, the inventions claimed in claims 11 to 13 (claims 11 to 14 after amendment) have been rewritten as indicated above; namely, "11. A semiconductor element wiring formed with the sputtered film of a copper alloy sputtering target containing 0.01 to (less than) 0.5wt% of at least 1 element selected from Al or Sn, and containing either Mn or Si or both in a total amount of 0.25wtppm or less" and "12. A semiconductor element wiring formed with the sputtered film of a copper alloy sputtering target containing 0.01 to (less than) 0.5wt% of at least 1 element selected from Al or Sn, and containing either Mn or Si or both in a total amount of 0.25wtppm or less; and further containing one or more selected from among Sb, Zr, Ti, Cr, Ag, Au, Cd, In and As in a total amount of 1.0wtppm or less" (claims 13 and 14 are omitted since they are dependent claims), and the constituent elements as substances, and not a manufacturing method, have been clarified.

Thereby, rejection B) above provided by the Examiner has been overcome.

Further, cited Document 1 and Document 2 do not in any way describe the

requirements of the inventions claimed in claims 11 to 14. This is because these claims are based on the primary constituent elements of claim 1 and claim 3, which have been acknowledged as possessing inventive step.

Accordingly, the inventions claimed in claims 11 to 14 are not identical to Document 1 and Document 2, nor can they be easily achieved based on Document 1 and Document 2.

4) Next, with respect to the rejection of C) above which states that although Comparative Example 4 is an invention pertaining to claim 1, the film thickness uniformity is not improved, there was a typographical error in Comparative Example 4, and although the Al content is 0.627wt%, it was erroneously indicated as 0.427wt%.

When the Al content is 0.627wt%, since it will obviously be outside the scope of claim 1, this should be described in the Comparative Examples as a matter of course. Nevertheless, the applicant should personally be responsible for such a typographical error, and this erroneous description has been deleted. Therefore, since the inconsistency concerning Comparative Example 4 has been eliminated, the rejection of foregoing C) has been overcome.

5) Next, with respect to the issue of D) above which states that the sheet resistance is not described in the Examples and Comparative Examples, the cause of the conductivity deteriorating (i.e., sheet resistance increasing) in a copper alloy containing trace elements is all alloy elements and impurities other than copper. This is described in detail on page 6 of the Description.

In other words, when the additive of amount of Al and Sn exceeds a

prescribed amount, when the additive amount of Mn and Si exceeds a prescribed amount, when the one or more elements selected from amount Sb, Zr, Ti, Cr, Ag, Au, Cd, In and As exceeds a prescribed amount, or when the inevitable impurities exceed a prescribed amount, all of these cases will increase the sheet resistance, and deteriorate the characteristics (sheet resistance) beyond the tolerable scope.

This is not a matter of being described in the Examples or Comparative Examples, and is a matter of being clearly explained and described in the Description. When the foregoing additives or impurities increase, unless an effect opposite of the present invention; for example, the fact that the sheet resistance will deteriorate or the verification thereof exists, there is no discrepancy in the present invention.

An invention is not only explained in the Examples or Comparative Examples. Since the present invention was sufficiently explained in the Description, no explanation was provided in the Examples and Comparative Examples.

Thus, the fact that the sheet resistance was not described in the Examples and Comparative Examples will not constitute grounds for the invention being insufficient or inadequate, and such perspective is a serious error.

6) As described above, the inventions described in Documents 1 and 2 do not in any way describe or suggest the present invention claimed in claims 1-16, and the technical spirit of the present invention and the technical spirited of Documents 1 and 2 are also clearly different. Thus, Documents 1 and 2 cannot be used as grounds to state that the present invention could have been easily achieved based

on such Documents 1 and 2. Further, typographical errors and discrepancies have been removed from the amended Description.

Accordingly, we request that the present invention be acknowledged as possessing patentability.